Next-Generation Semiconductors for DC-to-DC Converters

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Abstract. Recent developments in power devices for low voltage dc-to-dc conversion are discussed with emphasis on switch-mode dc-to-dc synchronous buck converter applications. The system functional blocks are presented and the progress in various devices such as power trench MOSFETs, Schottky barrier rectifiers, and power ICs is reviewed. The optimization of a new power trench MOSFET with W-shaped gate structure (WFET) as both a control and synchronous switch is investigated. The factors influencing system partitioning such as required performance, current level, power dissipation, and cost objectives are highlighted.

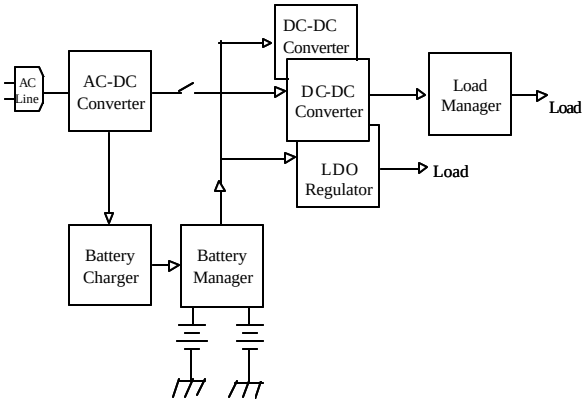
I. INTRODUCTION

The phenomenal increase in power demands of computing and telecommunications applications are driving rapid developments in semiconductor components for power conversion. [1]. Next-generation power devices need to address challenging future power requirements such as microprocessors with load currents in excess of 120 A, input voltages of about 1 V, and operating frequencies in 4 GHz range. In battery powered products such as notebook computers, cell phones, personal digital assistants (PDAs), MP3 players, and digital still cameras (DSCs), power devices need to be as efficient as possible as more features are added and expectations are raised for performance and miniaturization [2]. In addition to increased power levels, future products will require an increased number of regulated voltages and tighter power regulation that rely heavily on efficient power management systems.

Recent progress in power device technology has enabled the widespread use of distributed dc power management systems. These architectures offers the advantage of delivering several regulated localized supply rails with ease and the flexibility of selective subsystem shutdown [3]. A generic distributed architecture (Figure 1) includes the main functional blocks of voltage regulation and battery and load management. The broad function of voltage regulation includes both off-line (ac-to-dc), switchmode (dc-to-dc) converters and low dropout regulators (LDOs). The ac line supply of 115 V/220 V is rectified, filtered, and converted to a lower level supply rail, and/or it charges the battery. Power is supplied via a main power bus from an ac-to-dc converter or battery and feeds a number of dc-to-dc converters. Switchmode dc-to-dc converters provide higher efficiencies, particularly where a low output-to-input voltage ratio results from the widening gap between modern battery technology output voltages [4] and the operating voltages of future ULSI technology [5].

This paper discusses recent developments in power devices for low-voltage dc-to-dc conversion applications. Emphasis is placed on new device technologies for switch-mode dc-to-dc synchronous buck converters. The functional blocks of a switchmode dc-to-dc synchronous buck converter—including the PWM controller, power switches, and rectifier—are described. A review is presented of the progress made in various power devices, including trench MOSFETs, Schottky barrier rectifiers, and power ICs. The factors influencing system partitioning such as the required performance, current level, power dissipation, and cost objectives are highlighted.

DC-DC Converter Functional Blocks



The two topologies most commonly used as power stages for the distributed power architecture are the step-down (buck) converter and the step-up (boost) converter [6]. The output voltage of a four-cell Li-Ion battery pack, for example, will range from 16.8 V to 10 V during its discharge cycle. A buck converter can generate a steady 1.2-V supply rail from this variable battery voltage. On the other hand, a boost converter could be used to deliver a 13-V output voltage from the nominal 3.6-V input of a single-cell Li-Ion battery. This output voltage might be used to power three white LEDs in series, often the illumination source of color LCD displays in cell phones, PDAs and digital cameras.

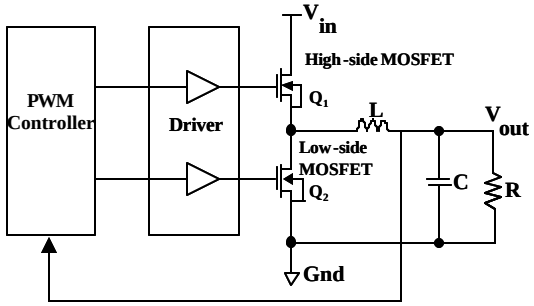


Figure 2. Circuit diagram of DC-DC Synchronous Buck Converter.

The synchronous buck converter shown in Figure 2 includes controller and driver functional blocks in conjunction with power high-side (control) switch (Q1), a low-side (synchronous) switch (Q2) to regulate the delivery of charge to the load, while L and C provide a filter. These converters are usually closed-loop systems where an output parameter like voltage or current is measured and compared with a reference value. The error signal is then utilized to control driving the switches. It is important to avoid power loss due to shoot-through [7], a condition where both transistors are conducting simultaneously. Therefore, the transistors must both be off while one is turning on and the other turning off. During this dead time, the intrinsic body diode of Q2 conducts current, which causes a high reverse-recovery charge Qrr [8]. In some applications, a Schottky diode is added to limit the intrinsic diode's forward voltage drop and reduce the power loss [9].

The topology shown in Figure 2 is for a single-phase converter. However, a multi-phase topology that interleaves parallel converters out of phase is utilized to meet the steady-state and transient response current requirements and to cancel output current ripple [10].

The system partitioning for low-voltage dc-to-dc converters depends to a great extent on the required current level, performance, and—obviously—cost. For high-current applications in the range of 100 A the usual choice is to design with separate controller-driver ICs, discrete power transistors, and Schottky diodes. For moderate current levels in the range of 20 A, single-package solutions continue to be developed [11]. For low- or medium-current applications in the range of 6 A, the controller-driver functions plus the power switches can be integrated into a single power IC [12]. In addition to the advantages of reduced size, a reduction in the number of external components brings about an expected performance improvement due to the elimination of parasitic inductances and capacitances.

II. POWER TRANSISTORS

Challenges to Trench MOSFET Scaling

MOSFETs are the main source of power losses in a buck converter and thus the best opportunity to improve efficiency performance. The MOSFET of choice for the

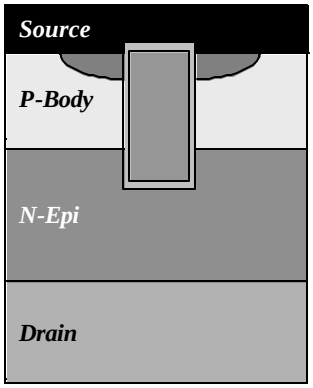


Figure 3. Schematic cross section of Conventional Trench MOSFET.

switches is the trench-gated U-groove MOSFET or UMOSFET [13], due to its ultra-low on-resistance.

Lower on-resistance is normally achieved by using higher cell density trench MOSFETs. This presents a challenge in scaling a conventional UMOSFET since its structure suffers from an inherent high overlap gate-drain or Miller capacitance C_{rss} (Figure 3). Since capacitance and on-resistance scale differently, a further increase in UMOSFET cell density is accompanied by a higher increase in C_{rss}, which degrades device switching performance. The Figure of Merit (FOM) used to evaluate the performance of these devices is the product of on-resistance and gate-drain charge $r_{DS(on)}*Q_{gd}$. Figure 4 shows the intrinsic limitations of scaling

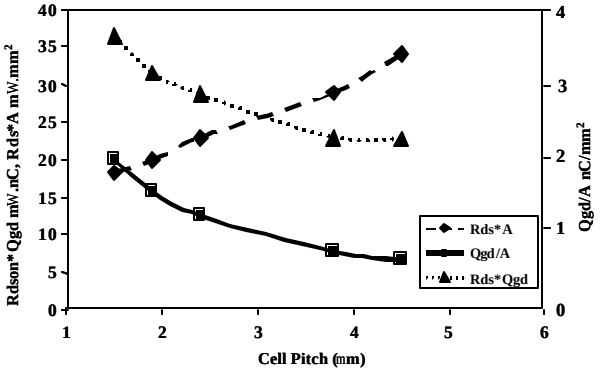


Figure 4. Figure of Merit Rds*Qgd vs. Cell Pitch of a UMOSFET Trench Width=0.6 µm.

conventional trench MOSFETs. The specific on-resistance Rds*A, the gate-drain charge per unit area Qgd/A and the the FOM $r_{DS(on)}$*Q_{gd} are plotted as a function of cell pitch. As the cell density increases, the specific on-resistance Rds*A decreases, however, the Qgd/A increases at a higher rate which results in a net increase in the FOM $r_{DS(on)}$*$Q_{gd.}$ A device with a 30-V breakdown voltage exhibits a minimum FOM $r_{DS(on)}$*Q_{gd} value of 35 mΩ.nC at a cell pitch of 4 µm. Further reductions of the cell pitch result in an undesirable increase in the $r_{DS(on)}$*Q_{gd} FOM. Therefore, a trade-off between the on-resistance and gate-drain charge sets the optimum value for cell density.

New Trench MOSFET Structures

To address this problem several approaches have been proposed. Lower gate-drain capacitance C_{rss} has been reported for MOSFETs with narrow trench width of 0.2 µm [14] or 0.15 µm [15] with a 1-µm cell pitch. Alternatively, to lower C_{rss} a thicker gate oxide was used on the walls of the trench [16-19]. To overcome several limitations of the above structures a new transistor with W-shaped gate trench MOSFET [20,21] (WFET™) has been recently reported and its cross section is shown in Figure 5.

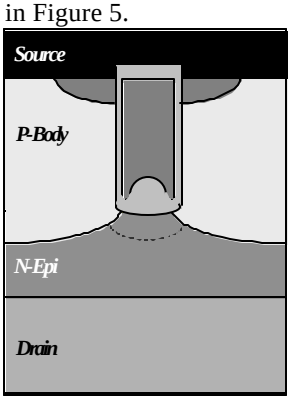


Figure 5. Schematic cross section of a W-Gated Trench MOSFET (WFET).

The WFET utilizes a thin gate oxide along the vertical walls and a thicker oxide at the bottom of the trench. The improvement over state-of-the-art structures is achieved by shaping the gate such that the thicker gate oxide at the bottom of the trench is self-aligned to the P-body / N-epi junction with a gradual transition to a thinner oxide along the trench walls and corners, resulting in a W-shaped gate. A slightly deeper P-body junction than the trench depth results in a lower capacitance as the source to drain voltage V_{DS} starts to increase. The WFET allows a further increase in cell density, for lower specific on-resistance, without sacrificing switching performance.

Devices were fabricated using a standard PWM-optimized Trench MOSFET process with an additional module [20,21]. A standard Trench MOSFET core process was used and the additional process module includes deposition of a nitride layer after the trench etch and pad oxide growth. The nitride layer is then removed only from the trench bottom. Self-alignment is achieved with a lightly doped arsenic implant at the bottom of the trench. A thick bottom oxide layer in the range of 100 - 200 nm is then realized by using a LOCOS process. The self–aligned arsenic implant minimizes the impact of the thicker oxide on on-resistance and provides a good process margin. Figure 6 shows a SEM cross-section of a W-gated Trench MOSFET (WFET) with a sidewall oxide of 30 nm and a thick bottom oxide of 150 nm. Using different gate oxide thickness provides an extra degree of freedom in optimizing WFETs compared to conventional device optimizations [22]. The choice of different sidewall and bottom gate oxide thickness values provides flexibility for a better specific on-resistance/gate charge trade-off. In the following section we examine WFET's optimization for use in dc-to-dc converters as both a control and/or a synchronous switch.

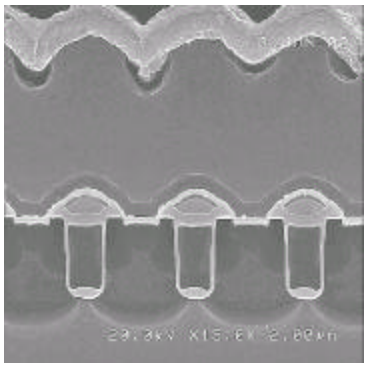


Figure 6. SEM crosses section of a W-Gated Trench MOSFET WFET.

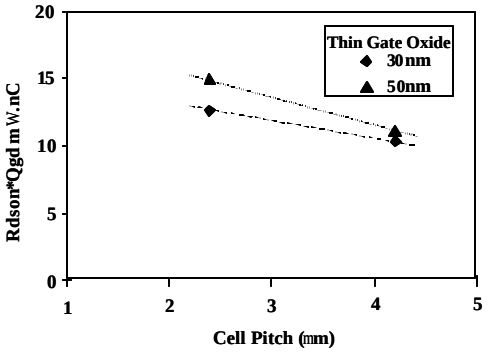


Figure 7. Figure of Merit $R_{ds}*Q_{gd}$ vs. cell pitch of a WFET.

Various device parameters such as cell pitch, gate oxide thickness, and trench depths were investigated. Fabricated devices using different cell pitches have a breakdown voltage greater than 35 V .

WFET OPTIMIZATION

In a synchronous buck converter, the power losses in the control MOSFET are given by equation (1) and are the sum of the losses due to conduction, switching, gate drive, and the loss associated with the output charge:

$$\mathbf{P}_{loss} = \mathbf{P}_{conduction}(r_{(DS)},I_{rms}) + \mathbf{P}_{switching}(Q_{gs},Q_{gd},V_{in},f) + \mathbf{P}_{drive}(Q_g,V_g,f) + \mathbf{P}_{output}(Q_{oss},V_{in},f) \quad (1)$$

where Q_{oss} is the output charge that must be supplied to the output capacitance and f is the switching frequency. In the control MOSFET conduction loss and switching loss are comparable. The requirement to minimize both conduction loss and switching loss highlights the need to use FOM $r_{DS(on)}*Q_{gd}$ in order to benchmark the performance of the control MOSFET. In addition, other device parameters that play an important role are the total gate charge Q_g and the threshold voltage Vth.

For the synchronous MOSFET, power losses are given by equation (2) and are due to conduction, gate drive, output, and losses associated with the body diode reverse recovery:

$$\mathbf{P}_{loss} = \mathbf{P}_{conduction}(R_{ds},I_{rms}) + \mathbf{P}_{drive}(Q_g,V_g,f) + \mathbf{P}_{output}(Q_{oss},Q_{rr},V_{in},f) \quad (2)$$

where Q_r is the body diode reverse-recovery stored charge. For the synchronous MOSFET the dominant component in power losses is conduction loss. Furthermore, the body diode conduction during the dead time period results in a stored charge Q_{rr}. To turn Q2 off, the stored charge Q_r needs to be removed, which results in power loss. Moreover, shoot-through or a high CdV/dt effect [7] may cause an additional power loss due to an undesired turn-on of the synchronous MOSFET. As can be seen from Figure 2, a rapid change in the drain voltage of Q2, resulting from the turn-on of Q1, may result in the turn-on of Q2. To avoid this effect, the ratio of Q_{gd}/Q_{gs} should be minimized in synchronous MOSFET, in addition to using a lower gate-resistance and an optimized threshold voltage Vth.

a) Control MOSFET

As a control switch, the WFET has a low $r_{DS(on)}*Q_{gd}$ FOM. This is a result of the significant reduction in WFET C_{rss} compared to a conventional device. A WFET with respective sidewall and bottom gate oxide thicknesses of 30 nm and 150 nm results in C_{rss} = 229 pF at V_{DS} = 0 V which is a factor of 3.7 lower than that of a conventional device having the same active area and cell pitch. The effect of cell pitch

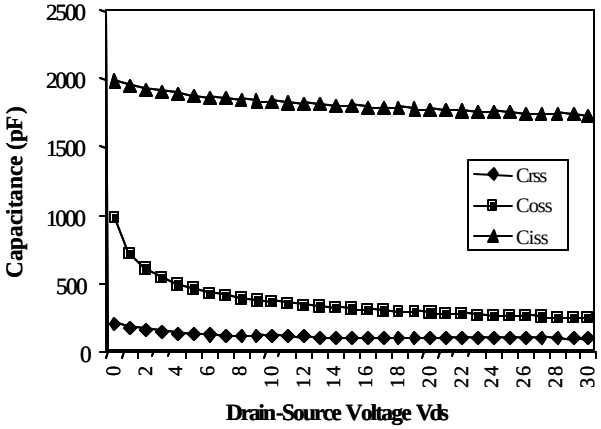


Figure 8.

on the figure of merit $r_{(DS)on}*Q_{gd}$ in a WFET is explored and the results are shown in Figure 7. The data shown are for WFET devices with different sidewall gate oxide thicknesses of 30 nm and 50 nm and a bottom oxide thickness of 150 nm. Different cell pitches varying from 2.4 µm to 4.2 µm were used. An increase in the cell pitch from 2.4 µm to 4.2 µm results in $r_{DS(on)}*Q_{gd}$ dropping from 12.5 mΩ.nC to about 10.5 mΩ.nC for the 30-nm device. This is due to the lower $r_{(DS)on}$ for the same Q_{gd} since the bottom oxide thickness and the channel width are the same. It is interesting to note that devices with a 30-nm sidewall oxide achieve a lower FOM $r_{(DS)on}*Q_{gd}$ than the 50-nm due to the lower on-resistance and similar Q_{gd}.

b) Synchronous MOSFET

The WFET can also be optimized for use as a synchronous switch. Using the 2.4-µm cell pitch, a cell

density higher than 100M cells/in^2 could be achieved. For a WFET with a cell pitch of 2.4 µm and sidewall and bottom gate oxide thicknesses of 50 nm and 180 nm respectively, the measured specific on-resistance is 22 mΩ.mm^2. The device exhibits a low Q_{gd}/Q_{gs} ratio, which is important for minimizing power loss due to shoot-through. The measured Q_{gd}/Q_{gs} ratio of a conventional PWM-optimized trench MOSFET was reduced from 0.8 to 0.45 for a WFET.

Figure 8 shows the same effect as an improvement in C_{rss} to the input capacitance C_{iss} ratio for a WFET with sidewall and bottom gate oxide thicknesses of 30 nm and 150 nm respectively. In the device optimization this improvement can be utilized to modify other important device parameters. For example, for the same shoot-through immunity, using a lower Q_{gd}/Q_{gs} ratio allows a lower threshold voltage V_{th} to be used. This approach results in reduced conduction loss and a lower total power loss.

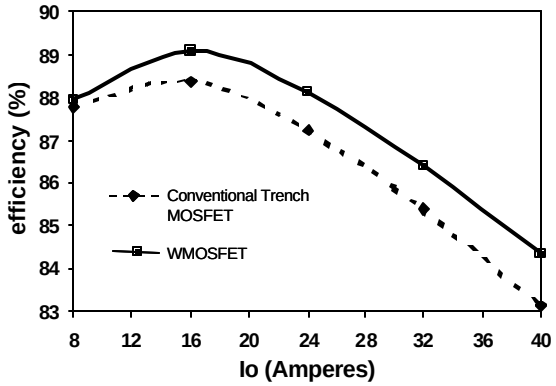


Figure 9. Measured efficiency vs. output current for a PWM switch-mode two-phase DC-DC Buck converter with 20V IN and 1.5V OUT.

c) Synchronous Buck DC-to-DC Converter Efficiency

The efficiency versus output current of a PWM switchmode, synchronous, two-phase, dc-to-dc buck converter with 12-V V_{IN} and 1.5-V V_{OUT} using WFET switches is shown in Figure 9. Using a switching frequency of 300 kHz, more than 91.5% efficiency could be achieved. Furthermore, efficiency at a full load of 40 A exceeds 85.5 %

.

The demonstrated higher efficiency of the WFET results from its low figure of merit FOM ($r_{DS(on)}$*Q_{gd}), low specific on-resistance ($r_{DS(on)}$*A), and higher shoot-through immunity due to its lower Q_{gd} and ratio of gate-drain to gate-source charges (Q_{gd}/Q_{gs}).

III. SCHOTTKY BARRIER RECTIFIER AND INTEGRATED MOSFET-SCHOTTKY SWITCH

As stated previously, during the dead time the intrinsic body diode of the MOSFET turns on and a high reverse recovery charge Qrr causes significant power loss. A low forward drop Schottky rectifier is therefore used to limit the turn-on of the body diode in the synchronous MOSFET Q2. Low forward drop Vf Schottky diodes use lower barrier heights that result in higher levels of leakage current [23]. However, reducing power loss requires minimizing reverse-biased Schottky diode leakage currents while maintaining high blocking voltages. Therefore, there is a tradeoff between the forward voltage drop Vf and the reverse bias leakage current I_L. The Trench MOS Schottky Barrier (TMBS) rectifier, as shown in Figure 10, allows the reduction of both V_f and I_L [24-27]. Under a reverse bias condition, the charge coupling between the charges in the drift

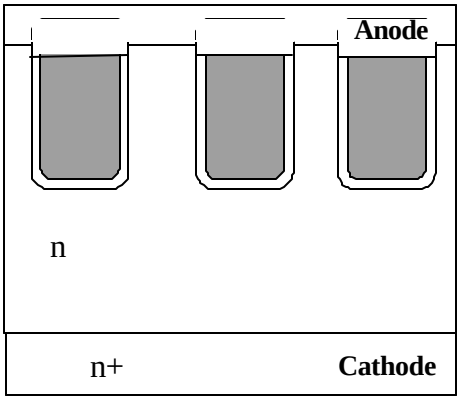


Figure 10. Cross section of a Trench MOS Schottky Barrier (TMBS).

region and the adjacent MOS structure depletes the drift

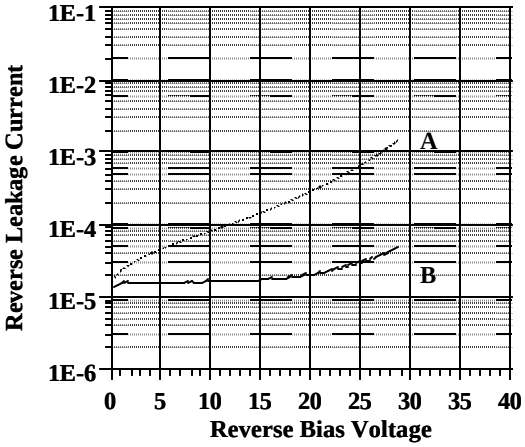


Figure 11. Leakage current vs. reverse bias voltage for a palaner Schottky (A) and a TMBS (B).

region. This results in the reduction of the electric field at the center of the Schottky contact compared to the ideal planar rectifier. Therefore, a significant reduction in the leakage current is realized (see Figure [11]). This effect allows the use of a lower barrier metal to achieve lower V_f for an acceptable, slightly higher leakage current. It should be noted that the reduced barrier lowering effect leads to a flat blocking characteristic, but the onset of the leakage current at a low anode voltage is determined by the Schottky barrier height and the doping of the semiconductor at the contact [28]. The optimization of barrier metal, mesa width, trench depth, epitaxial layer thickness, and oxide thickness are key to device performance. TMBS reported results show 40 mV lower V_f and a factor of 4 reduction in the leakage current compared to a planar device with the same breakdown voltage and current carrying capability [26].

A monolithically integrated trench power MOSFET and TMBS diode [29] exploits the synergy between trench MOSFET and TMBS devices to achieve improved performance. The cross section of such a structure is shown in Figure 12, where TMBS cells are distributed within the trench MOSFET cells. For the synchronous switch an integrated device provides improved reverse recovery speed performance by eliminating the external wiring between the MOSFET and the Schottky diode. This results in reduced parasitic resistance, inductance,

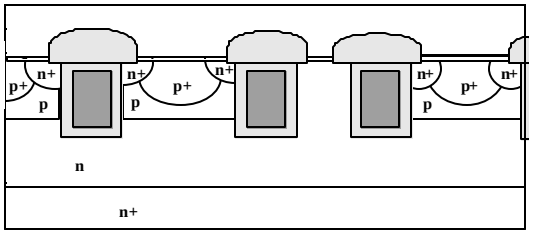


Figure 12. A cross section of a monolithically.

and EMI/RFI, particularly at high frequencies.

V. BCDMOS IC TECHNOLOGY

Achieving the maximum benefit in low- and medium-power applications leads to the integration of the digital cores, analog, and power devices into a single IC. This enables the design of a complete dc-to-dc converter system using only few external components. Bipolar CMOS-DMOS (BCDMOS) technologies have been developed to address these needs in multi-voltage and mixed-signal integrated circuits [30]. Using BCDMOS technology allows the integration of the controller-driver functions together with the power transistors on the same die. In addition to its obvious performance advantages this approach further facilitates distributed power or Point of Load (POL) architectures. Furthermore, advanced control techniques such as zero-voltage switching (ZVS), and adaptive and predictive drive techniques, can be readily used to minimize power loss during dead time [31].

In a mixed-analog BCDMOS technology the device arsenal usually includes 3.3 V, 5 V CMOS for digital blocks, 12 V CMOS for analog functions, and Lateral DMOS (LDMOS) [32] or quasi-vertical planar [6]or trench power transistors [33]. The use of deep trench isolation [34] and the more conventional junction isolation enables the technology to include complementary high-performance NPN and quasi-vertical PNP transistors. The process can be dual gate oxide, multiple poly, and 3 to 4 levels of metal. The top level metal is a thick power metal for lower on-resistance. An example of such a process [12] uses 15-µm CuNiPd top metal and achieves specific on-resistance of 36 $m\Omega.mm^2$ at V_{GS} = 5 V for an n-channel device with a 17-V breakdown voltage. Also of significance for analog circuits is the development BCDMOS technology with flash memory [35] and one-time programmable (OTP) EPROM cells for post-package trimming [1].

Figure 13 shows the functional building blocks of a high-performance synchronous buck converter with dynamically adjustable output voltage [36]. The chip has both control and synchronous switches and a low voltage section that includes the digital and analog circuitry needed for power device control, gate drive, voltage mode PWM comparator, high-speed error amplifier, oscillator, and voltage reference. The MOSFETs switch at a high frequency of 2 MHz to minimize the area taken by the magnetic components. The output current is sensed internally.

Figure 14 shows a photomicrograph of the IC shown in Figure 13, where low on-resistance 0.25 Ω control and synchronous switches occupy about 40% of the total die area.

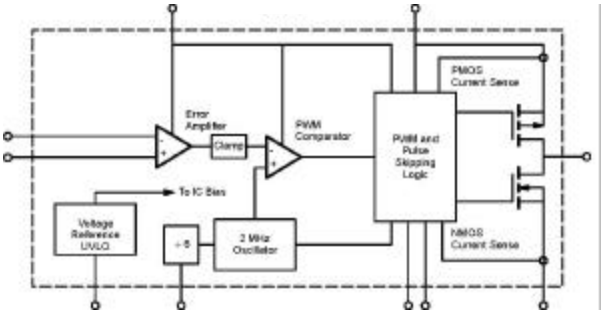


Figure 13. Functional block diagram of an integrated

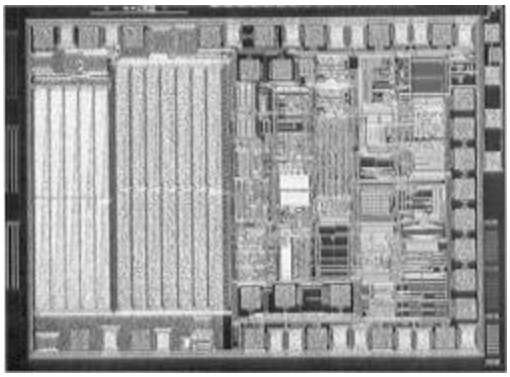


Figure 14. Photomicrograph of an integrated switch-mode dc-dc buck converter.

IX. Summary

A new generation of power devices has been developed to meet evolving dc-to-dc power conversion requirements. Progress made in power trench MOSFETs and Schottky barrier rectifiers designed for low voltage switchmode dc-to-dc synchronous buck converters offer significant performance advantages. Optimization of W-shaped gate trench MOSFETs (WFET) provides attractive control and synchronous switch characteristics. Developments in Bipolar-CMOS-DMOS technology enable the integration of a complete dc-to-dc converter in a single chip. Power devices and mixed-signal BCDMOS technologies offer designers a wide array of system partitioning options.

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